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DECLARATION

I, Michie Fuse-Ofuchi , a Patent Attorney, of Ogikubo TM Bldg. 2F, 5-26-13, Ogikubo, Suginami-ku, Tokyo 167-0051, Japan, solemnly and sincerely declare:

That I have a thorough knowledge of Japanese and English languages; and

That the attached pages contain a correct translation into English of the specification of the following Japanese Patent Application:

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Michie Fuse-Ofuchi

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[Name of Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE, MEMORY SYSTEM AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] A semiconductor device provided with a memory cell including a first load transistor, a second load transistor, a first driver transistor, a second driver transistor, a first transfer transistor and a second transfer transistor, the semiconductor device comprising:

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively.

[Claim 2] The semiconductor device according to claim 1,

wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, and

wherein the second drain-gate wiring layer is electrically connected to the second

gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

[Claim 3] The semiconductor device according to claim 1 or 2, wherein the first drain-gate wiring layer is located in a layer lower than the second drain-gate wiring layer.

[Claim 4] The semiconductor device according to any one of claims 1 to 3, wherein the first drain-gate wiring layer is located in a layer in which the first gate-gate electrode layer is provided.

[Claim 5] The semiconductor device according to any one of claims 1 to 4, wherein the second drain-gate wiring layer is formed across a plurality of layers.

[Claim 6] The semiconductor device according to claim 5,

wherein the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

[Claim 7] The semiconductor device according to claim 6, wherein the upper layer is electrically connected to the lower layer through a contact section.

[Claim 8] The semiconductor device according to claim 6 or 7,

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer,

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer, and

wherein the upper layer is located in a third conductive layer.

[Claim 9] The semiconductor device according to any one of claims 1 to 13, wherein the second conductive layer is titanium nitride.

[Claim 10] The semiconductor device according to any one of claims 1 to 9, wherein the second conductive layer has a thickness of 100 nm to 200 nm.

[Claim 11] A memory system provided with the semiconductor device defined in any one of claims 1 to 10.

[Claim 12] An electronic apparatus provided with the semiconductor device defined in any one of claims 1 to 10.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to semiconductor devices, such as, for example, static random access memories (SRAMs), and memory systems and electronic apparatuses provided with the same.

[0002]

[Background Art]

SRAMs, one type of semiconductor memory devices, do not require a refreshing operation and therefore have a property that can simplify the system and lower power consumption. For this reason, the SRAMs are prevailingly used as memories for electronic equipment, such as, for example, mobile phones.

[0003]

[Problems to be Solved by the Invention]

The objective of the present invention is to provide a semiconductor device that can reduce its cell area.

[0004]

Another objective of the present invention is to provide a memory system and an electronic apparatus that includes a semiconductor device of the present invention.

[0005]

[Means for Solving the Problems]

(Semiconductor Device)

A semiconductor device in accordance with the present invention is provided with a memory cell including a first load transistor, a second load transistor, a first driver transistor, a second driver transistor, a first transfer transistor and a second transfer transistor, the semiconductor device comprising:

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively.

[0006]

Here, the "wiring layer" means a conductive layer disposed over a field or an interlayer dielectric layer.

[0007]

In accordance with the present invention, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, in accordance with the present invention, the pattern density of a wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area can be made smaller, compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

[0008]

The semiconductor device of the present invention may take at least any one of the following features.

[0009]

(a) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, and

the second drain-gate wiring layer may be electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

[0010]

(b) The first drain-gate wiring layer may be located in a layer lower than the second drain-gate wiring layer.

[0011]

(c) The first drain-gate wiring layer may be located in a layer in which the first gate-gate electrode layer is provided.

[0012]

(d) The second drain-gate wiring layer may be formed across a plurality of layers.

[0013]

In this feature, the second drain-gate wiring layer may include a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

the upper layer may be located in a layer over the lower layer, and electrically connected to the lower layer.

[0014]

Further, in this feature, the upper layer may be electrically connected to the lower layer through a contact section.

[0015]

Further, in this feature, the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first conductive layer,

the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and

the upper layer may be located in a third conductive layer.

[0016]

(e) The second conductive layer may be a nitride layer of a refractory metal. As the second conductive layer is a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniaturizing processing can be readily performed. Accordingly, the cell area can be reduced.

[0017]

(f) The second conductive layer may have a thickness of 100 nm to 200 nm.

[0018]

(Memory System)

A memory system in accordance with the present invention is provided with the semiconductor device as defined in any one of claims 1 to 10.

[0019]

(Electronic Apparatus)

An electronic apparatus in accordance with the present invention is provided with the semiconductor device as defined in any one of claims 1 to 10.

[0020]

[Embodiments]

An embodiment of the present invention is described. The present embodiment is the one in which a semiconductor device of the present invention is applied to in an SRAM.

[0021]

[Equivalent Circuit of SRAM]

Fig. 1 is an equivalent circuit diagram of an SRAM in accordance with the present embodiment. The SRAM of the present embodiment is a type in which one memory cell is formed with six MOS field effect transistors. In other words, one CMOS inverter is formed with an n-channel type driver transistor Q3 and a p-channel type load transistor Q5. Also, one CMOS inverter is formed with an n-channel type driver transistor Q4 and a p-channel type load transistor Q6. These two CMOS inverters are cross-coupled to form a flip-flop. Further, one memory cell is formed from this flip-flop and n-channel type transfer transistors Q1 and Q2.

[0022]

[Structure of SRAM]

A structure of the SRAM is described below. First, each figure is briefly described.

[0023]

Fig. 2 schematically shows a plan view of a field of the memory cell of the SRAM in accordance with the present embodiment. Fig. 3 schematically shows a plan view of a first conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 4 schematically shows a plan view of a second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 5 schematically shows a plan view of a third conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 6 schematically shows a plan view of a fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 7 schematically shows a plan view of the field and the first conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 8 schematically shows a plan view of the field and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 9 schematically shows a plan view of the first conductive layer and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 10 schematically shows a plan view of the second conductive layer and the third conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 11 schematically shows a plan view of the third conductive layer and the fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 12 schematically shows a cross-sectional view taken along a line A-A shown in Fig. 2 to Fig. 11. Fig. 13 schematically shows a cross-sectional view taken along a line B-B shown in Fig. 2 to Fig. 11.

[0024]

(Field and First conductive layer)

Referring to Fig. 2, the field is described. The field includes first through fourth active regions 14, 15, 16 and 17 and an element isolation region 12. The first through fourth active

regions 14, 15, 16 and 17 are defined by the element isolation region 12. A region on the side where the first and second active regions 14 and 15 are formed is an n-type well region W10, and a region on the side where the third and fourth active regions 16 and 17 are formed is a p-type well region W20.

[0025]

The first active region 14 and the second active region 15 are disposed in a symmetrical relation in a planar configuration. Also, the third active region 16 and the fourth active region 17 are disposed in a symmetrical relation in a planar configuration.

[0026]

P^+-type impurity layers 14a and 14b are formed in the first active region 14. In the first active region 14, a load transistor Q5 is formed.

[0027]

P^+-type impurity layers 15a and 15b are formed in the second active region 15. In the second active region 15, a load transistor Q6 is formed.

[0028]

In the third active region 16, n^+-type impurity layers 16a, 16b and 16c that are to become components of the transistors Q1 and Q3 are formed. In the third active region 16, a p^+-type impurity layer 16d that composes a well contact region is formed. In the third active region 16, a driver transistor Q3 and a transfer transistor Q1 are formed.

[0029]

In the fourth active region 17, n^+-type impurity layers 17a, 17b and 17c that are to become components of the transistors Q2 and Q4 are formed. In the fourth active region 17, a p^+-type impurity layer 17d that composes a well contact region is formed. In this fourth active region 17, a driver transistor Q4 and a transfer transistor Q2 are formed.

[0030]

Next, referring to Fig. 3 and Fig. 7, the first conductive layer is described referring to the physical relationship between the first conductive layer and the field.

[0031]

The first conductive layer includes a first gate-gate electrode layer 20, a second gate-gate electrode layer 22, a first drain-gate wiring layer 30 and an auxiliary word line 24. For example, the first conductive layer may be formed by successively depositing a polysilicon layer and a silicide layer in layers.

[0032]

The first gate-gate electrode layer 20 and the second gate-gate electrode layer 22 are formed in a manner to extend along a Y direction. The first drain-gate wiring layer 30 and the auxiliary word line 24 are formed in a manner to extend along an X direction.

[0033]

The first gate-gate electrode layer 20 is formed in a manner to traverse the first active region 14 and the third active region 16. The first gate-gate electrode layer 20 functions as a gate electrode of the load transistor Q5 and the driver transistor Q3. The first drain-gate wiring layer 30 is formed in a manner to extend in the X direction from a side section of the first gate-gate electrode layer 20 between the first active region 14 and the third active region 16 toward the second gate-gate electrode layer 22.

[0034]

The second gate-gate electrode layer 22 is formed in a manner to traverse the second active region 15 and the fourth active region 17. The second gate-gate electrode layer 22 functions as a gate electrode of the load transistor Q6 and the driver transistor Q4.

[0035]

The auxiliary word line 24 is formed in a manner to traverse the third active region 16 and the fourth active region 17. The auxiliary word line 24 functions as a gate electrode of the transfer transistors Q1 and Q2.

[0036]

The physical relationship between the first conductive layer and the impurity layers formed in the active regions is described below.

[0037]

A p^+-type impurity layer 14a and a p^+-type impurity layer 14b are formed so that the first

gate-gate electrode layer 20 is located between the p^+-type impurity layer 14a and the p^+-type impurity layer 14b. In other words, the p^+-type impurity layer 14a, the p^+-type impurity layer 14b, and the first gate-gate electrode layer 20 form the load transistor Q5. The p^+-type impurity layer 14a forms a source of the load transistor Q5, and the p^+-type impurity layer 14b forms a drain of the load transistor Q5.

[0038]

A p^+-type impurity layer 15a and a p^+-type impurity layer 15b are formed so that the second gate-gate electrode layer 22 is located between the p^+-type impurity layer 15a and the p^+-type impurity layer 15b. In other words, the p^+-type impurity layer 15a, the p^+-type impurity layer 15b, and the second gate-gate electrode layer 22 form the load transistor Q6. The p^+-type impurity layer 15a forms a source of the load transistor Q6, and the p^+-type impurity layer 15b forms a drain of the load transistor Q6.

[0039]

An n^+-type impurity layer 16b and an n^+-type impurity layer 16c are formed so that the first gate-gate electrode layer 20 is located between the n^+-type impurity layer 16b and the n^+-type impurity layer 16c. In other words, the n^+-type impurity layer 16b, the n^+-type impurity layer 16c, and the first gate-gate electrode layer 20 form the driver transistor Q3. The n^+-type impurity layer 16b forms a drain of the driver transistor Q3, and the n^+-type impurity layer 16c forms a source of the driver transistor Q3.

[0040]

An n^+-type impurity layer 17b and an n^+-type impurity layer 17c are formed so that the second gate-gate electrode layer 22 is located between the n^+-type impurity layer 17b and the n^+-type impurity layer 17c. In other words, the n^+-type impurity layer 17b, the n^+-type impurity layer 17c, and the second gate-gate electrode layer 22 form the driver transistor Q4. The n^+-type impurity layer 17b forms a drain of the driver transistor Q4, and the n^+-type impurity layer 17c forms a source of the driver transistor Q4.

[0041]

An n^+-type impurity layer 16a and an n^+-type impurity layer 16b are formed so that the

auxiliary word line 24 is located between the n^+-type impurity layer 16a and the n^+-type impurity layer 16b. In other words, the n^+-type impurity layer 16a, the n^+-type impurity layer 16b, and the auxiliary word line 24 form the transfer transistor Q1. The n^+-type impurity layer 16b forms a source or a drain of the transfer transistor Q1, and the n^+-type impurity layer 16a forms a source or a drain of the transfer transistor Q1.

[0042]

An n^+-type impurity layer 17a and an n^+-type impurity layer 17b are formed so that the auxiliary word line 24 is located between the n^+-type impurity layer 17a and the n^+-type impurity layer 17b. In other words, the n^+-type impurity layer 17a, the n^+-type impurity layer 17b, and the auxiliary word line 24 form the transfer transistor Q2. The n^+-type impurity layer 17a forms a source or a drain of the transfer transistor Q2, and the n^+-type impurity layer 17b forms a source or a drain of the transfer transistor Q2.

[0043]

P^+-type impurity layers 16d and 17d form a well contact region of a p well.

[0044]

An interlayer dielectric layer 90 is formed so as to cover the field and the first conductive layer (see Figs. 12 and 13). The interlayer dielectric layer 90 may be formed through a planarization process utilizing, for example, a chemical mechanical polishing method.

[0045]

(Second Conductive Layer)

Referring to Fig. 4, Fig. 8 and Fig. 9, the second conductive layer is described below.

[0046]

The second conductive layer includes, a first drain-drain wiring layer 40, a second drain-drain wiring layer 42, a lower layer 32a of the second drain-gate wiring layer, a first BL contact pad layer 70a, a first bar-BL contact pad layer 72a, a first Vss contact pad layer 74a and a Vdd contact pad layer 76.

[0047]

The first drain-drain wiring layer 40, the second drain-drain wiring layer 42 and the

lower layer 32a of the second drain-gate wiring layer are formed in a manner to extend in the Y direction.

[0048]

The first drain-drain wiring layer 40 has portions that overlap the first active region 14 and the third active region 16 as viewed in a plan view (see Fig. 8). More concretely, one end portion 40a of the first drain-drain wiring layer 40 is located above the p^+-type impurity layer 14b. The one end portion 40a of the first drain-drain wiring layer 40 and the p^+-type impurity layer 14b are electrically connected to each other through a contact section between the field and the second conductive layer (herein blew referred to as a "field/second-layer contact section") 80. The other end portion 40b of the first drain-drain wiring layer 40 is located above the second n^+-type impurity layer 16b. The other end portion 40b of the first drain-drain wiring layer 40 and the n^+-type impurity layer 16b are electrically connected to each other through the field/second-layer contact section 80.

[0049]

The second drain-drain wiring layer 42 has portions that overlap the second active region 15 and the fourth active region 17 as viewed in a plan view (see Fig. 8). More concretely, one end portion 42a of the second drain-drain wiring layer 42 is located above the p^+-type impurity layer 15b. The one end portion 42a of the second drain-drain wiring layer 42 and the p^+-type impurity layer 15b are electrically connected to each other through the field/second-layer contact section 80. The other end portion 42b of the second drain-drain wiring layer 42 is located above the n^+-type impurity layer 17b. The other end portion 42b of the second drain-drain wiring layer 42 and the n^+-type impurity layer 17b are electrically connected to each other through the field/second-layer contact section 80.

[0050]

Further, the second drain-drain wiring layer 42 has a portion that overlaps an end portion 30a of the first drain-gate wiring layer 30 as viewed in a plan view (see Fig. 9). The second drain-drain wiring layer 42 and the end portion 30a of the first drain-gate wiring layer 30 are electrically connected to each other through a contact section between the first conductive layer

and the second conductive layer (hereafter referred to as a "first-layer/second-layer contact section") 82.

[0051]

The lower layer 32a of the second drain-gate wiring layer is formed on the opposite side of the first drain-drain wiring layer 40 with respect to the second drain-drain wiring layer 42 as being a reference. The lower layer 32a of the second drain-gate wiring layer has a portion that overlaps the second gate-gate electrode layer 22 as viewed in a plan view (see Fig. 9). The lower layer 32a of the second drain-gate wiring layer, and the second gate-gate electrode layer 22 are electrically connected to each other through the first-layer/second-layer contact section 82.

[0052]

The first BL contact pad layer 70a is located above the n^+-type impurity layer 16a in the third active region 16 (see Fig. 8). The first BL contact pad layer 70a and the n^+-type impurity layer 16a are electrically connected to each other through the field/second-layer contact section 80.

[0053]

The first bar-BL contact pad layer 72a is located above the n^+-type impurity layer 17a in the fourth active region 17 (see Fig. 8). The first bar-BL contact pad layer 72a and the n^+-type impurity layer 17a are electrically connected to each other through the field/second-layer contact section 80.

[0054]

The first Vss contact pad layers 74a are located above the sources of the n^+-type impurity layer 16c and the p^+-type impurity layer 16d in the third active region 17 (see Fig. 8). Each of the first Vss contact pad layers 74a is electrically connected to the n^+-type impurity layer 16c through the field/second-layer contact section 80. Also, the first Vss contact pad layer 74a is electrically connected to the p^+-type impurity layer 16d through the field/second-layer contact section 80. The first Vss contact pad layers 74a is commonly used by memory cells adjacent each other in the X direction in Fig. 8.

[0055]

Each of the Vdd contact pad layers 76 is located above the p^+-type impurity layer 14a in

the first active region 14. Each of the Vdd contact pad layers 76 is electrically connected to the p^+-type impurity layer 14a through the field/second-layer contact section 80.

[0056]

Next, a cross-sectional structure of the second conductive layer is described with reference to Fig. 12 and Fig. 13. The second conductive layer may be formed only from, for example, a nitride layer of a refractory metal. The thickness of the second conductive layer may be for example 100 nm to 200 nm, and more specifically be 140 nm to 160 nm. The nitride layer of a refractory metal may be formed from, for example, titanium nitride. Because the second conductive layer is formed from a nitride layer of a refractory metal, the thickness of the second conductive layer can be made smaller, and miniature processing thereof can be readily conducted. Accordingly, the cell area can be reduced.

[0057]

Also, the second conductive layer may be composed in either one of the following embodiments. 1) It may have a structure in which a nitride layer of a refractory metal is formed on a metal layer formed from a refractory metal. In this case, the metal layer formed from a refractory metal is an under-layer, and may be composed of a titanium layer, for example. Titanium nitride may be listed as a material of the nitride layer of a refractory metal. 2) The second conductive layer may be composed only of a metal layer of a refractory metal.

[0058]

Next, a cross-sectional structure of the field/second-layer contact section 80 is described with reference to Fig. 12 and Fig. 13. The field/second-layer contact section 80 is formed in a manner to fill a through hole 90a that is formed in the interlayer dielectric layer 90. The field/second-layer contact section 80 includes a barrier layer 80a, and a plug 80b formed over the barrier layer 80a. Titanium and tungsten may be listed as material of the plugs. The barrier layer 80a may be formed from a metal layer of a refractory metal, and a nitride layer of a refractory metal formed over the metal layer. For example, titanium may be listed as material of the metal layer of a refractory metal. Titanium nitride, for example, may be listed as material of the nitride layer of a refractory metal.

[0059]

Next, a cross-sectional structure of the first-layer/second-layer contact section 82 is described with reference to Fig. 12 and Fig. 13. The first-layer/second-layer contact section 82 is formed in a manner to fill a through hole 90b that is formed in the first interlayer dielectric layer 90. The first-layer/second-layer contact section 82 may have the same structure as that of the field/second-layer contact section 80 described above.

[0060]

A second interlayer dielectric layer 92 is formed in a manner to cover the second conductive layer. The second interlayer dielectric layer 92 may be formed through a planarization process using, for example, a chemical mechanical polishing method.

[0061]

The third conductive layer is described below with reference to Fig. 5 and Fig. 10.

[0062]

The third conductive layer includes an upper layer 32b of the second drain-gate wiring layer, a main word line 50, a Vdd wiring 52, a second BL contact pad layer 70b, a second bar-BL contact pad layer 72b and a second Vss contact pad layer 74b.

[0063]

The upper layer 32b of the second drain-gate wiring layer, the main word line 50 and the Vdd wiring 53 are formed in a manner to extend along the X direction.

[0064]

The upper layer 32b of the second drain-gate wiring layer is formed in a manner to traverse the second drain-drain wiring layer 42 in the second conductive layer, as shown in Fig. 10. More concretely, the upper layer 32b of the second drain-gate wiring layer is formed from an area above the end portion 40b of the first drain-drain wiring layer 40 to an area above an end portion 32a1 of the lower layer 32a of the second drain-gate wiring layer. The upper layer 32b of the second drain-gate wiring layer is electrically connected to the end portion 40b of the first drain-drain wiring layer 40 through a contact section between the second conductive layer and the third conductive layer (herein after referred to as a "second-layer/third-layer contact section") 84.

Also, the upper layer 32b of the second drain-gate wiring layer is electrically connected to the end portion 32a1 of the lower layer 32a of the second drain-gate wiring layer through the second-layer/third-layer contact section 84.

[0065]

The Vdd wiring 52 is formed in a manner to pass over the Vdd contact pad layer 76. The Vdd wiring 52 is electrically connected to the Vdd contact pad layer 76 through the second-layer/third-layer contact section 84. The Vdd wiring 52 is commonly used by memory cells adjacent each other in the Y direction in Fig. 10.

[0066]

The second BL contact pad layer 70b is located above the first BL contact pad layer 70a. The second BL contact pad layer 70b is electrically connected to the first BL contact pad layer 70a through the second-layer/third-layer contact section 84.

[0067]

The second bar-BL contact pad layer 72b is located above the first bar-BL contact pad layer 72a. The second bar-BL contact pad layer 72b is electrically connected to the first bar-BL contact pad layer 72a through the second-layer/third-layer contact section 84.

[0068]

The second Vss contact pad layer 74b is located above the second Vss contact pad layer 74a. The second Vss contact pad layer 74b is electrically connected to the first Vss contact pad layer 74a through the second-layer/third-layer contact section 84.

[0069]

Next, a cross-sectional structure of the third conductive layer is described with reference to Fig. 12 and Fig. 13. The third conductive layer has a structure in which, for example, a nitride layer of a refractory metal, a metal layer, and a nitride layer of a refractory metal, in this order from the bottom, are successively stacked in layers. For example, titanium nitride may be listed as material of the nitride layer of a refractory metal. Aluminum, copper or an alloy of these metals, for example, may be listed as material of the metal layer.

[0070]

Next, referring to Figs. 12 and 13, a cross-sectional structure of the second-layer/third-layer contact section 84 is described. The second-layer/third-layer contact section 84 is formed in a manner to fill a through hole 92a formed in the interlayer dielectric layer 92. The second-layer/third-layer contact section 84 may be provided with the same structure as that of the field/second-layer contact section 80 described above.

[0071]

A third interlayer dielectric layer 94 is formed in a manner to cover the third conductive layer. The interlayer dielectric layer 94 may be formed through a planarization process using, for example a chemical mechanical polishing method.

[0072]

(Fourth Conductive Layer)

The fourth conductive layer is described below with reference to Fig. 6 and Fig. 11.

[0073]

The fourth conductive layer includes a bit line 60, a bit-bar line 62 and a Vss wiring 64.

[0074]

The bit line 60, the bit-bar line 62 and the Vss wiring 64 are formed in a manner to extend along the Y direction.

[0075]

The bit line 60 is formed in a manner to pass over the second BL contact pad layer 70b. The bit line 60 is electrically connected to the second BL contact pad layer 70b through a contact section between the third conductive layer and the fourth conductive layer (herein below referred to as a "third-layer/fourth-layer contact section") 86.

[0076]

The bit-bar line 62 is formed in a manner to pass over the second bar-BL contact pad layer 72b. The bit-bar line 62 is electrically connected to the second bar-BL contact pad layer 72b through the third-layer/fourth-layer contact section 86.

[0077]

The Vss wiring 64 is formed in a manner to pass over the second Vss contact pad layer

74b. The Vss wiring 64 is electrically connected to the second Vss contact pad layer 74b through the third-layer/fourth-layer contact section 86.

4) Cross-Sectional Structure of Fourth Conductive Layer

[0078]

Next, a cross-sectional structure of the fourth conductive layer is described with reference to Fig. 12 and Fig. 13. The fourth conductive layer may have the same structure as the structure of the third conductive layer described above.

[0079]

Next, referring to Figs. 12 and 13, a cross-sectional structure of the third-layer/fourth-layer contact section 86 is described. The third-layer/fourth-layer contact section 86 is formed in a manner to fill a through hole 94a that is formed in the interlayer dielectric layer 94. The third-layer/fourth-layer contact section 86 may have the same structure as the structure of the field/second-layer contact section 80 described above.

[0080]

Although not shown in Fig. 12 or Fig. 13, a passivation layer may be formed on the fourth conductive layer.

[0081]

[Effects]

Effects provided by the semiconductor device in accordance with the present embodiment are described below.

[0082]

A first drain-gate wiring layer and a second drain-gate wiring layer could be formed in the same conductive layer. However, in this case, it is difficult to reduce the cell area due to the high pattern density of the conductive layer where the first and second drain-gate wiring layers are formed.

[0083]

However, in accordance with the present embodiment, the first drain-gate wiring layer 30 is located in the first conductive layer. Also, the second drain-gate wiring layer has a structure

that is divided into the lower layer 32a of the second drain-gate wiring layer and the upper layer 32b of the second drain-gate wiring layer. The lower layer 32a of the second drain-gate wiring layer is located in the second conductive layer, and the upper layer 32b of the second drain-gate wiring layer is located in the third conductive layer. Consequently, the first drain-gate wiring layer and the second drain-gate wiring layer are formed in different layers, respectively. Accordingly, since the first drain-gate wiring layer and the second drain-gate wiring layer are not formed in the same layer, the pattern density of the wiring layer can be reduced. Therefore, by the memory cell in accordance with the present embodiment, the cell area can be reduced.

[0084]

[Example of Application of SRAM to Electronic Equipment]

The SRAM in accordance with the present embodiment may be applied to electronic equipment, such as, for example, mobile equipment. Fig. 14 shows a block diagram of a part of a mobile telephone system. A CPU 540, an SRAM 550 and a DRAM 560 are mutually connected via a bus line. Further, the CPU 540 is connected to a keyboard 510 and an LCD driver 520 via the bus line. The LCD driver 520 is connected to a liquid crystal display section 530 via the bus line. The CPU 540, the SRAM 550 and the DRAM 560 compose a memory system.

[0085]

Fig. 15 shows a perspective view of a mobile telephone 600 that is provided with the mobile telephone system shown in Fig. 14. The mobile telephone 600 is equipped with a main body section 610 including a keyboard 612, a liquid crystal display section 614, a receiver section 616 and an antenna section 618, and a lid section 620 including a transmitter section 622.

[0086]

The present invention is not limited to the embodiment described above, and a variety of modifications can be made within the scope of the subject matter of the present invention.

[Brief Description of the Drawings]

[Fig.1]

Fig. 1 is an equivalent circuit diagram of an SRAM in accordance with the present

embodiment.

[Fig.2]

Fig. 2 schematically shows a plan view of a field of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.3]

Fig. 3 schematically shows a plan view of a first conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.4]

Fig. 4 schematically shows a plan view of a second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.5]

Fig. 5 schematically shows a plan view of a third conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.6]

Fig. 6 schematically shows a plan view of a fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.7]

Fig. 7 schematically shows a plan view of the field and the first conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.8]

Fig. 8 schematically shows a plan view of the field and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.9]

Fig. 9 schematically shows a plan view of the first conductive layer and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.10]

Fig. 10 schematically shows a plan view of the second conductive layer and the third conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.11]

Fig. 11 schematically shows a plan view of the third conductive layer and the fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.12]

Fig. 12 schematically shows a cross-sectional view taken along a line A-A shown in Fig. 2 to Fig. 11.

[Fig.13]

Fig. 13 schematically shows a cross-sectional view taken along a line B-B shown in Fig. 2 to Fig. 11.

[Fig.14]

Fig. 14 shows a block diagram of a part of a mobile telephone system provided with the SRAM in accordance with the present embodiment.

[Fig.15]

Fig. 15 shows a perspective view of a mobile telephone that is provided with the mobile telephone system shown in Fig. 14.

[Explanation of Reference Numerals]

10 silicon substrate

12 element isolation region

14 first active region

14a, 14b p^+-type impurity layer

15 second active region

15a, 15b p^+-type impurity layer

16 third active region

16a, 16b, 16c n^+-type impurity layer

16d p^+-type impurity layer

17 fourth active region

17a, 17b, 17c n^+-type impurity layer

17d p^+-type impurity layer

20	first gate-gate electrode layer
22	second gate-gate electrode layer
24	auxiliary word line
30	first gate-drain wiring layer
32a	lower layer of second gate-drain wiring layer
32b	upper layer of second gate-drain wiring layer
40	first drain-drain wiring layer
42	second drain-drain wiring layer
50	main word line
52	Vdd wiring
60	bit line
62	bit-bar line
64	Vss wiring
70a	first BL contact pad layer
70b	second BL contact pad layer
72a	first bar-BL contact pad layer
72b	second bar-BL contact pad layer
74a	first Vss contact pad layer
74b	second Vss contact pad layer
76	Vdd contact pad layer
80	field/second-layer contact section
82	first-layer/second-layer contact section
84	second-layer/third-layer contact section
86	third-layer/fourth-layer contact section
90	interlayer dielectric layer
90a	through hole
92	interlayer dielectric layer
92a	through hole

94	interlayer dielectric layer
94a	through hole
Q1	first transfer transistor
Q2	second transfer transistor
Q3	first driver transistor
Q4	second driver transistor
Q5	first load transistor
Q6	second load transistor

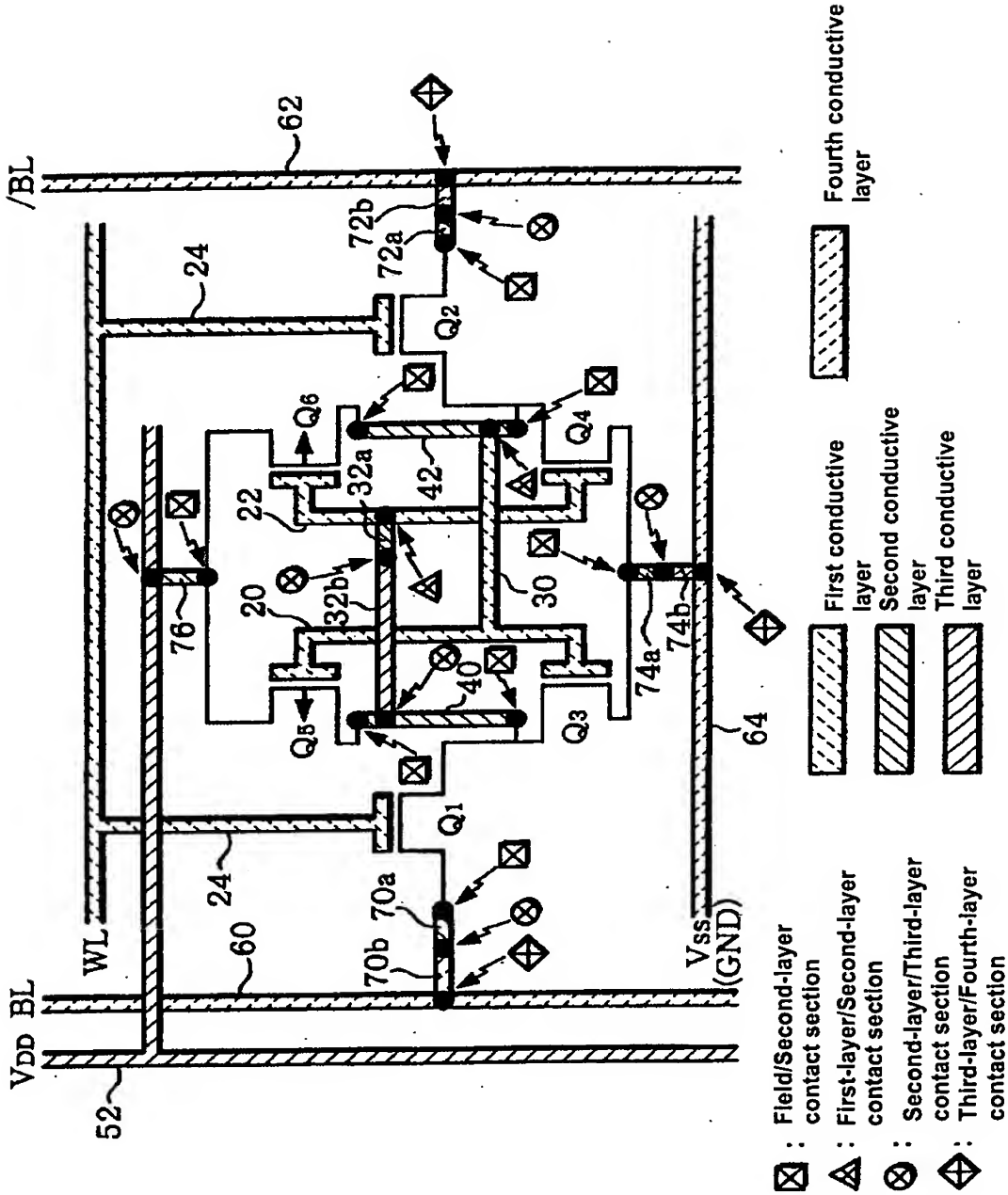

/BL
WL
BL
VDD
Vss (GND)
Q1
Q2
Q3
Q4
Q5
Q6
20
22
24
30
32a
32b
40
42
52
60
62
64
70a
70b
72a
72b
74a
74b
76
Fourth conductive layer
First conductive layer
Second conductive layer
Third conductive layer
: Field/Second-layer contact section
: First-layer/Second-layer contact section
: Second-layer/Third-layer contact section
: Third-layer/Fourth-layer contact section

Fig. 1

Fig. 2

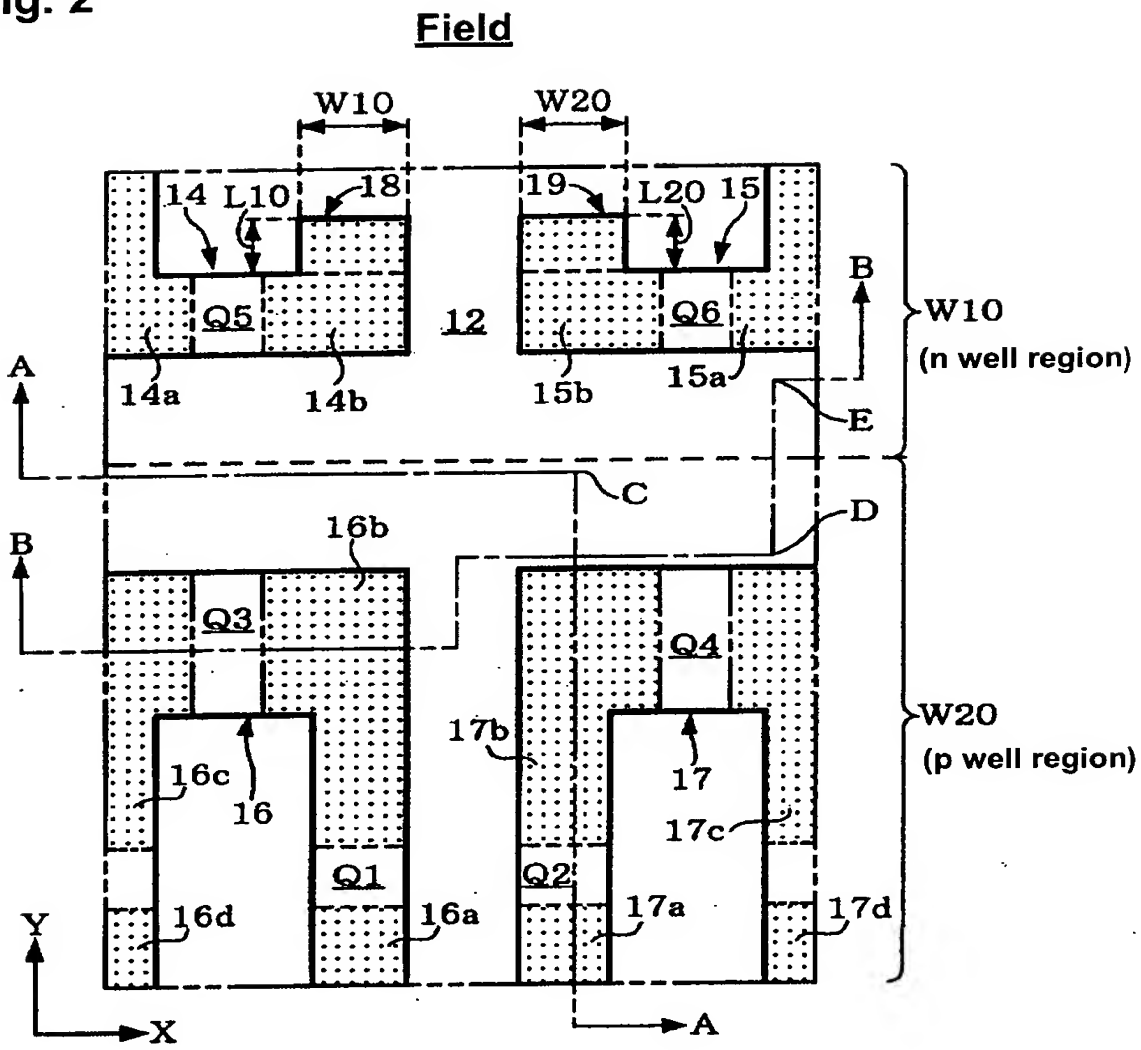

Field
W10
W20
14
L10
18
19
L20
15
B
W10
(n well region)
Q5
12
Q6
A
14a
14b
15b
15a
E
C
D
16b
B
Q3
Q4
W20
(p well region)
17b
16c
16
17
17c
Q1
Q2
16d
16a
17a
17d
Y
X
A

Fig. 3

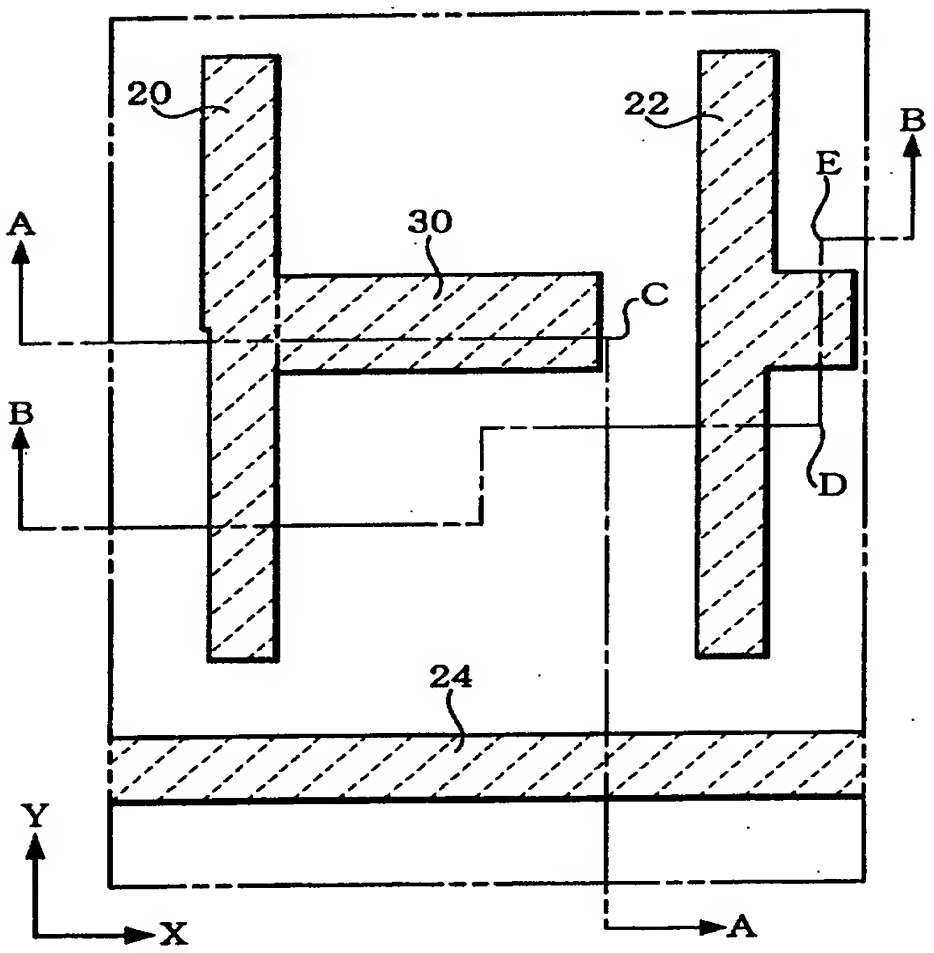


Fig. 4

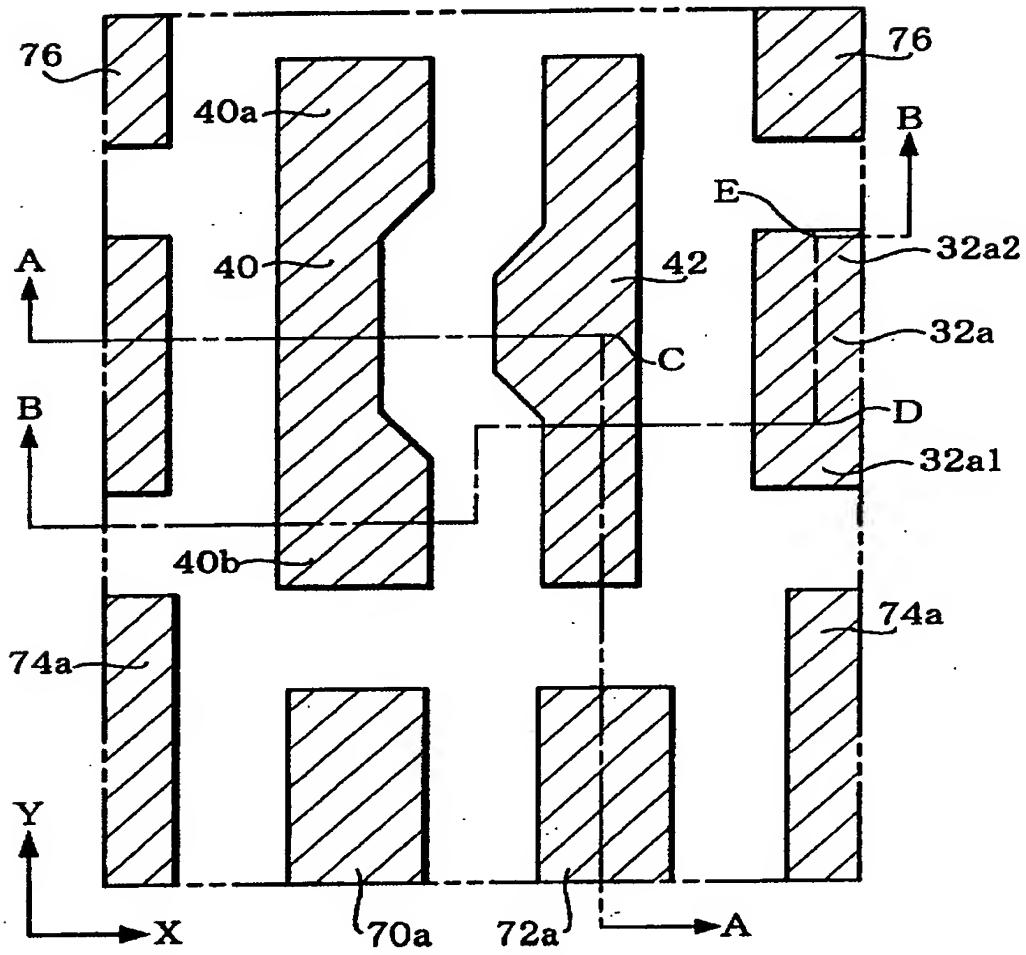

Second conductive layer
76
40a
76
B
E
A
40
42
32a2
32a
C
B
D
32a1
40b
74a
74a
Y
X
70a
72a
A

Fig. 5

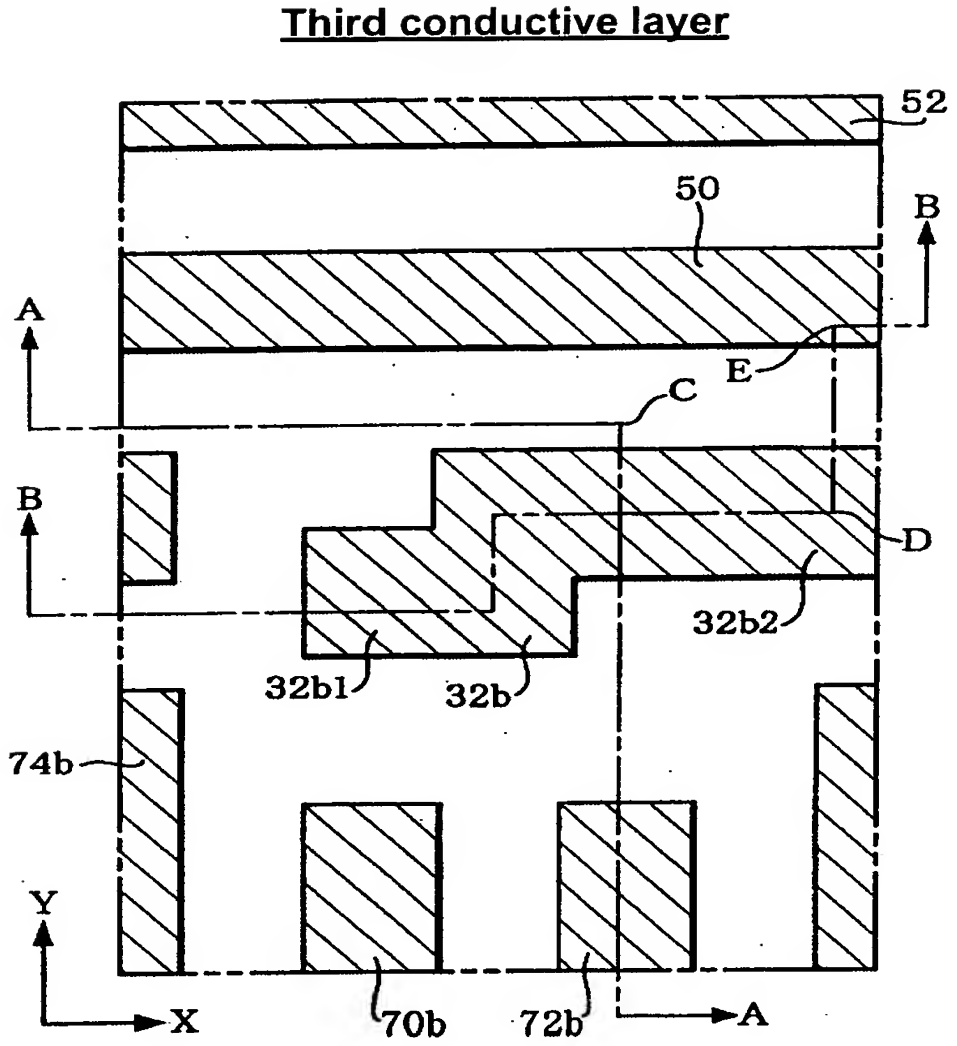

Third conductive layer
52
50
B
A
E
C
B
D
32b2
32b1
32b
74b
Y
X
70b
72b
A

Fig. 6

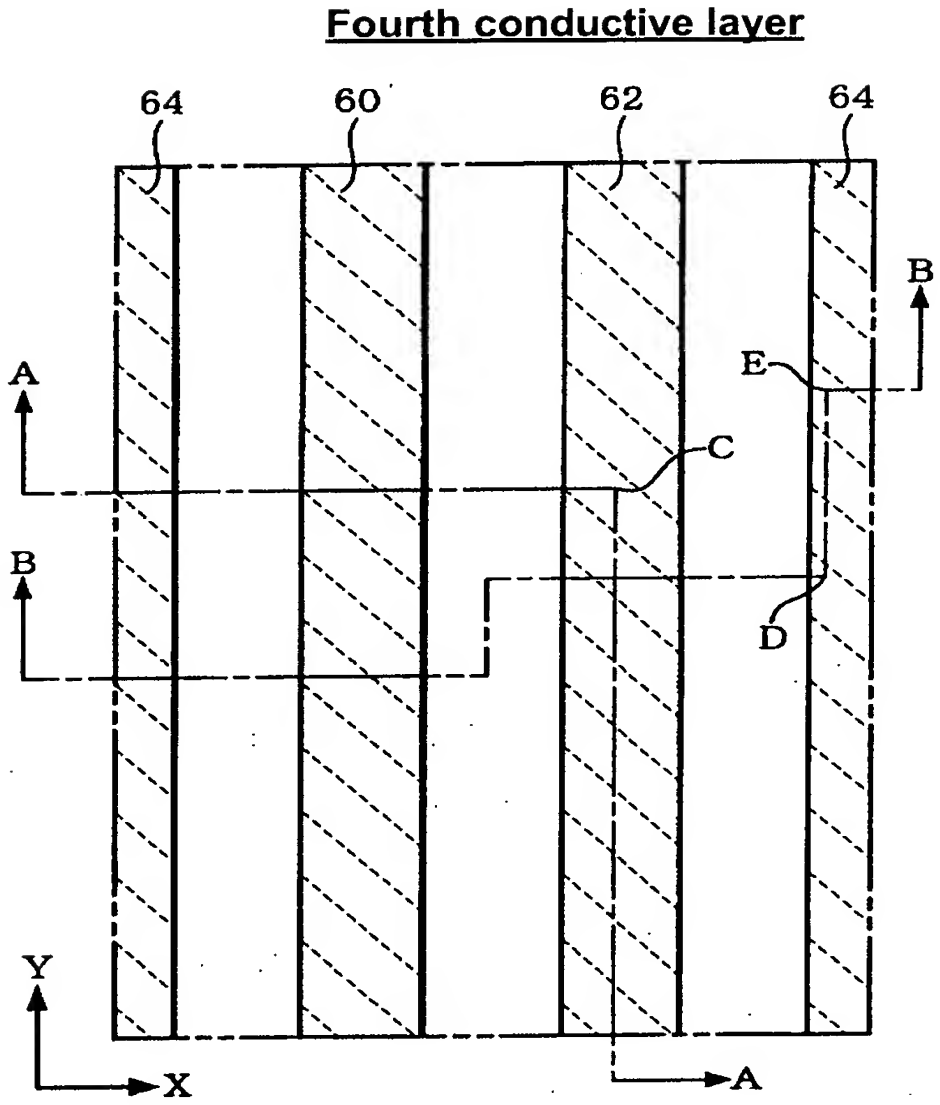


Fig. 7

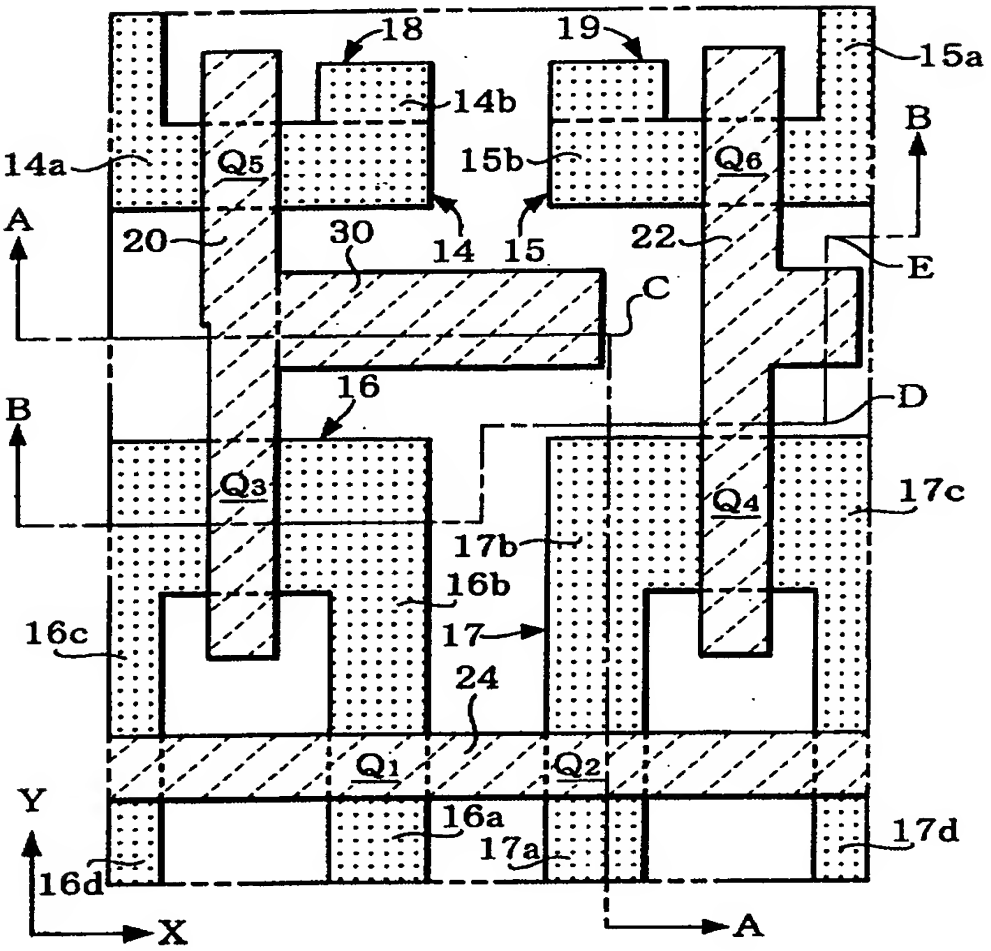

Field / First conductive layer
18
19
15a
14b
B
14a
Q5
15b
Q6
A
20
30
14
15
22
E
C
16
D
B
Q3
Q4
17c
17b
16b
16c
17
24
Q1
Q2
Y
16a
17d
17a
16d
X
A

Fig. 8

Field / Second conductive layer

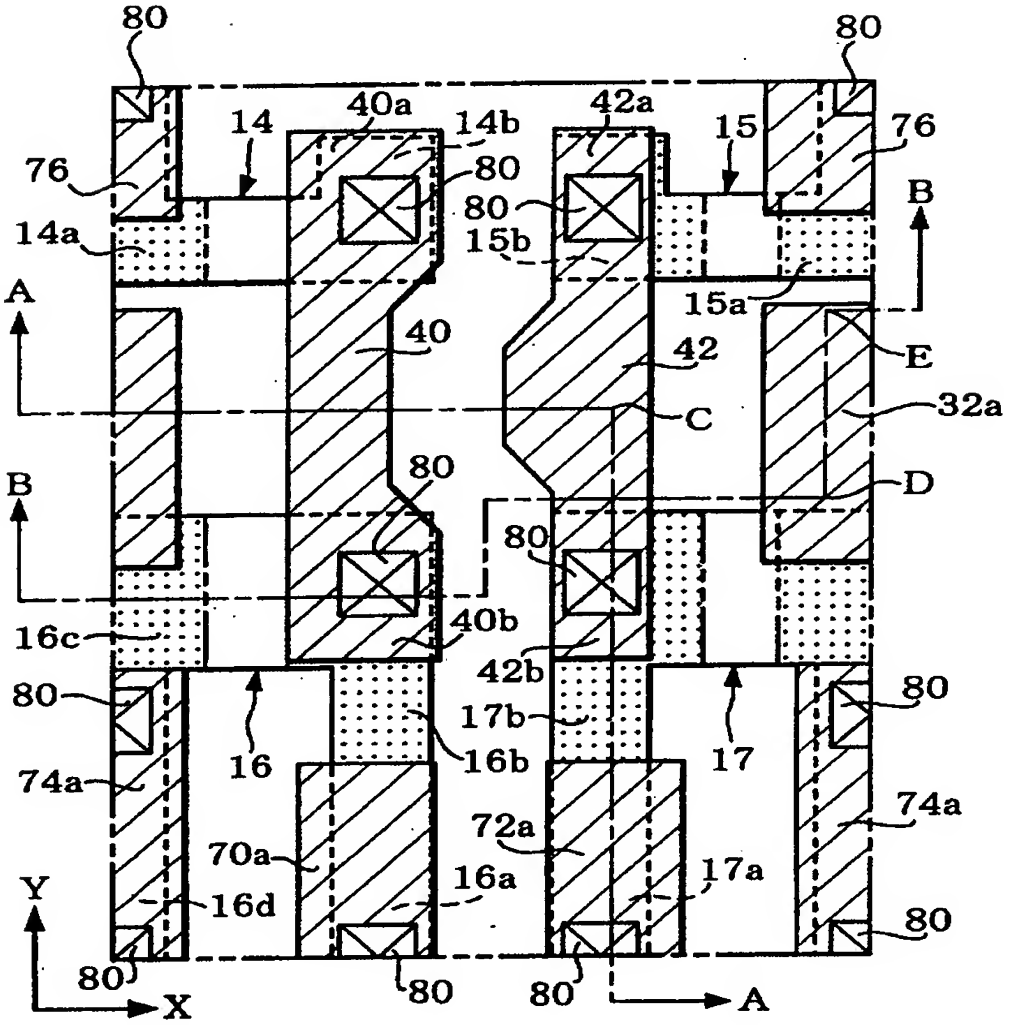


Fig. 9

First conductive layer / Second conductive layer

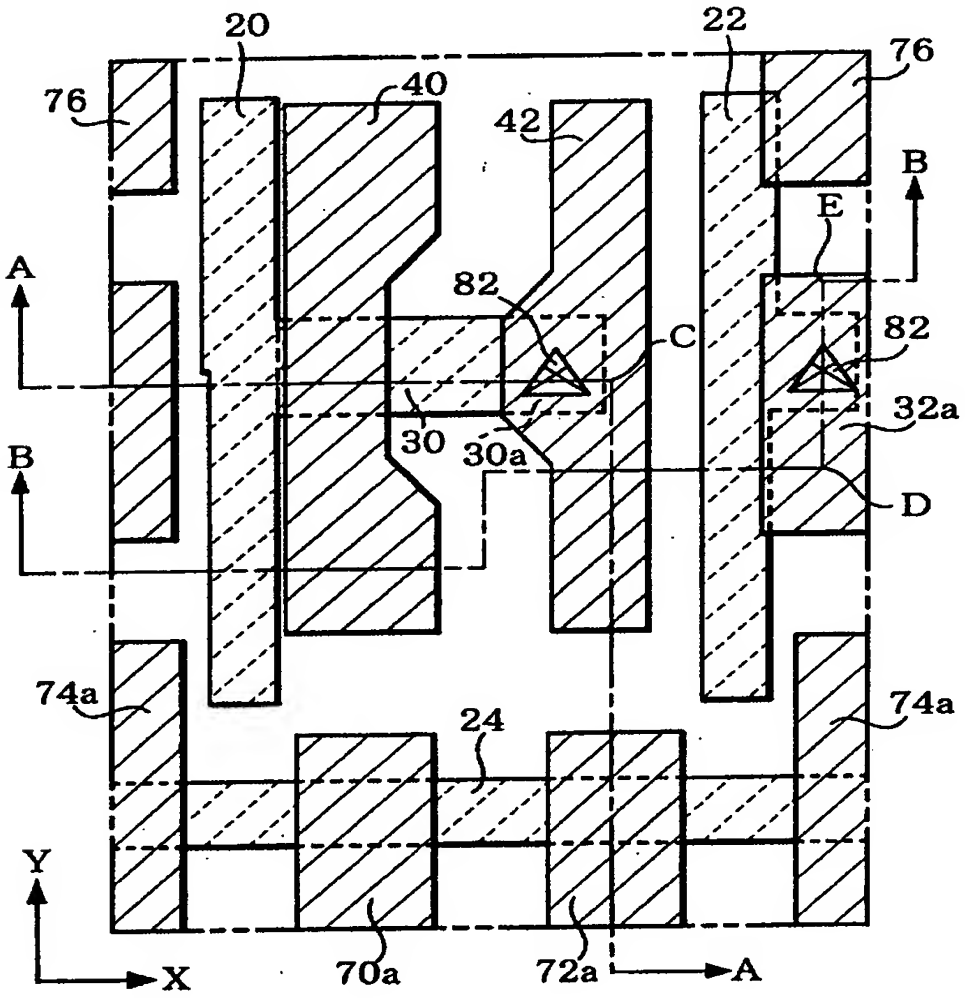


Fig. 10

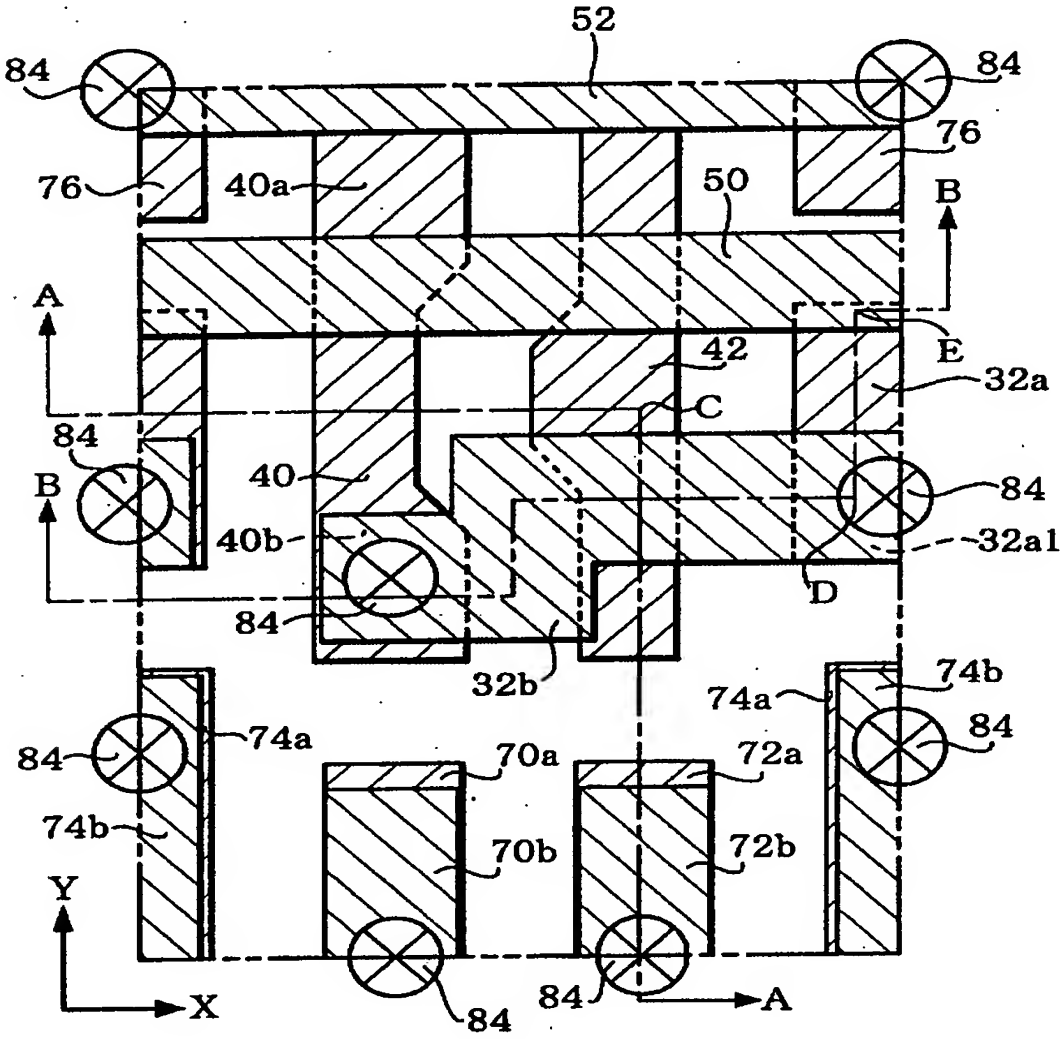
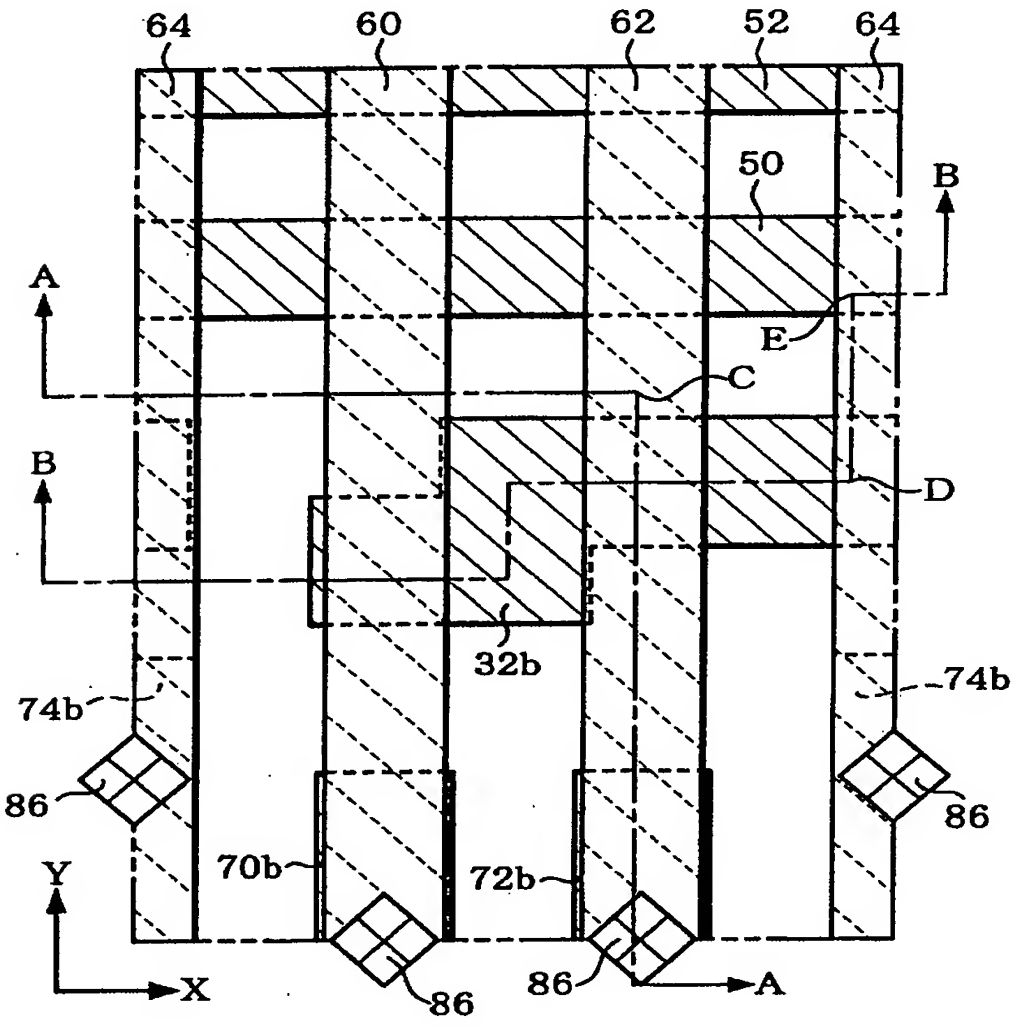

Second conductive layer / Third conductive layer
52
84
84
76
76
40a
50
B
A
42
E
32a
C
84
40
84
B
40b
32a1
84
D
32b
74b
74a
84
74a
84
70a
72a
74b
70b
72b
Y
X
84
84
A

Fig. 11


Third conductive layer / Fourth conductive layer
64
60
62
52
64
50
B
A
E
C
B
D
32b
74b
74b
86
86
70b
72b
Y
X
86
86
A

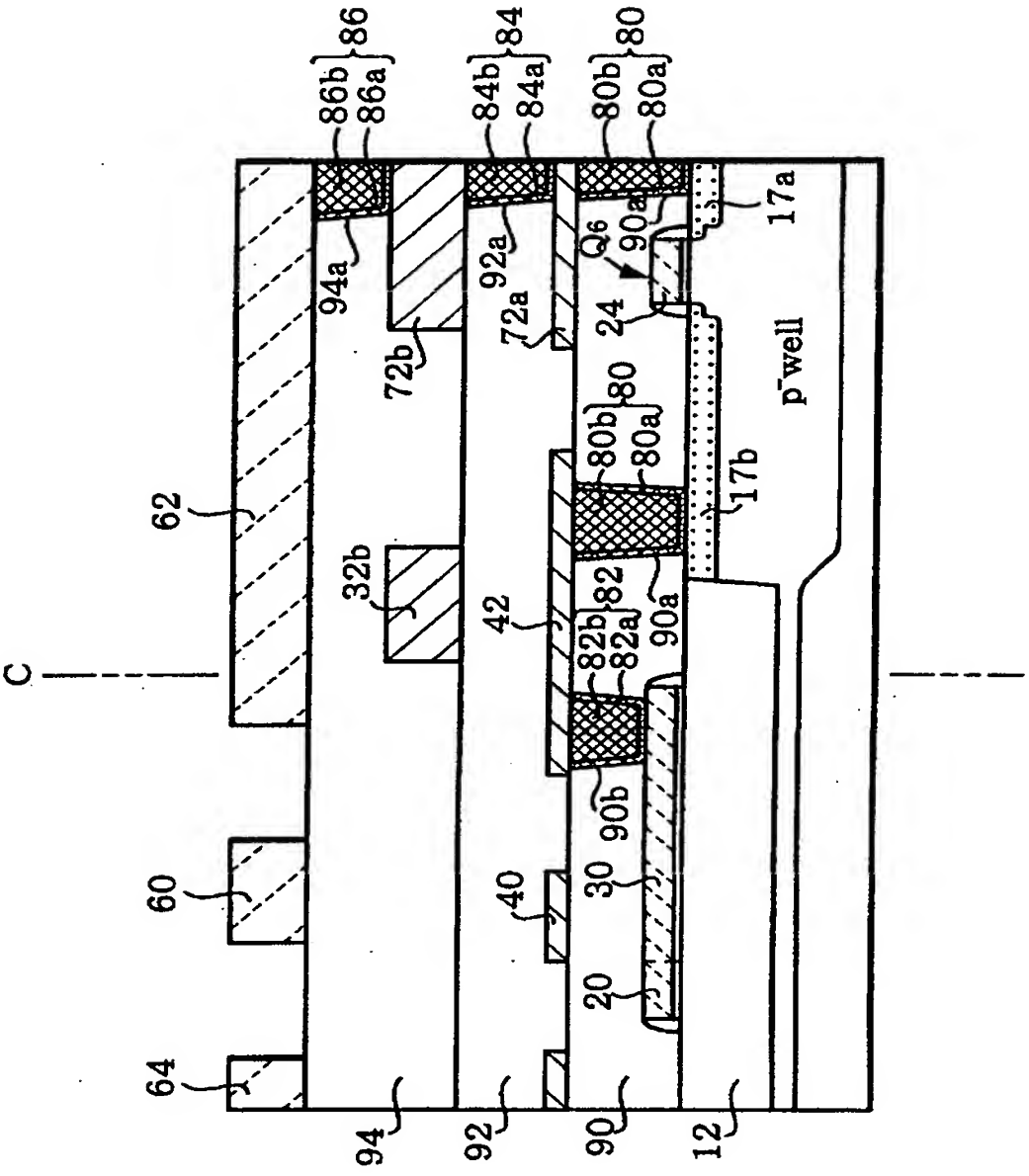

86b
86a
86
84b
84a
84
80b
80a
80
17a
Q6
90a
94a
92a
72a
24
72b
p⁻well
80b
80a
80
17b
62
32b
82
42
82b
82a
90a
C
90b
60
30
40
20
64
94
92
90
12

Fig. 12

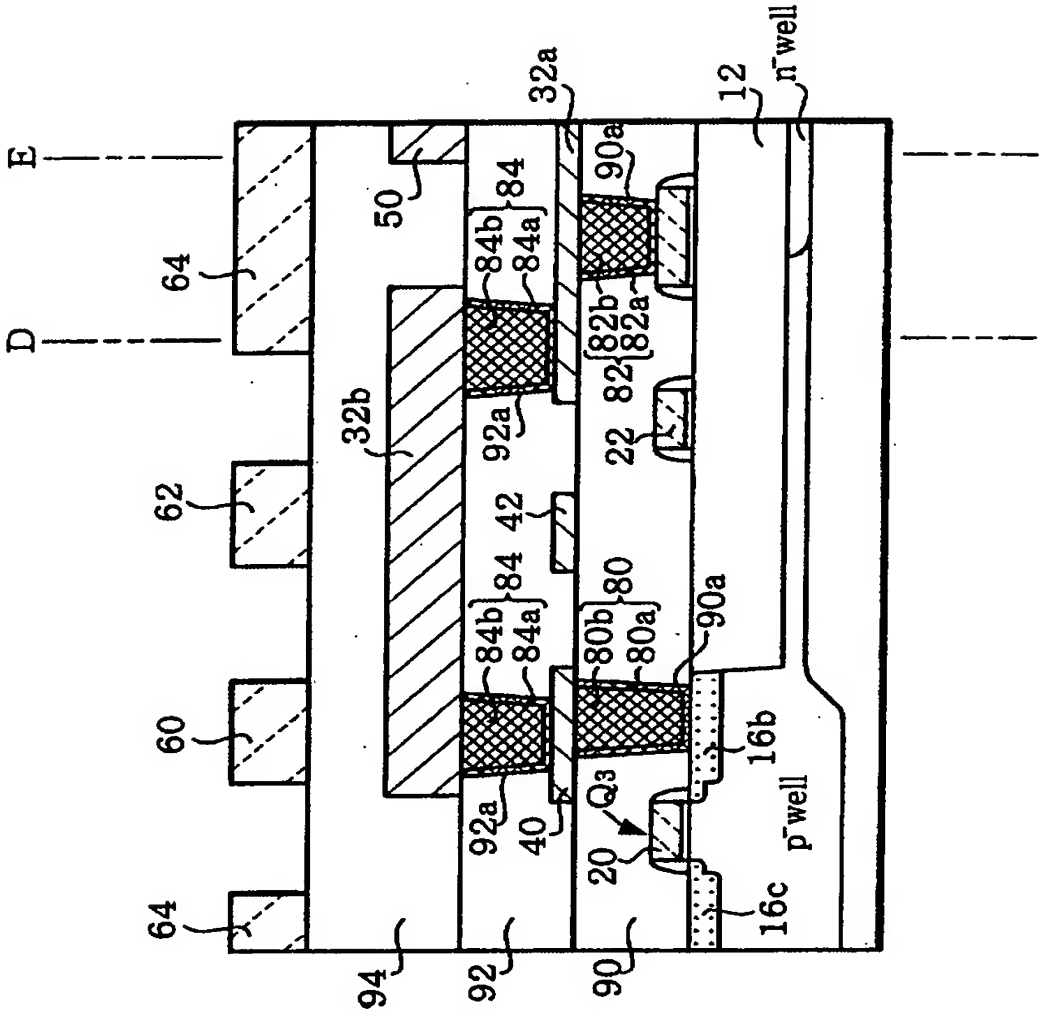

E
D
64
62
60
64
50
32a
32b
12
n⁻well
84
84b
84a
90a
82
82b
82a
22
92a
42
80
80b
80a
40
Q3
20
16b
16c
p⁻well
94
92
90

Fig. 13

Fig. 14

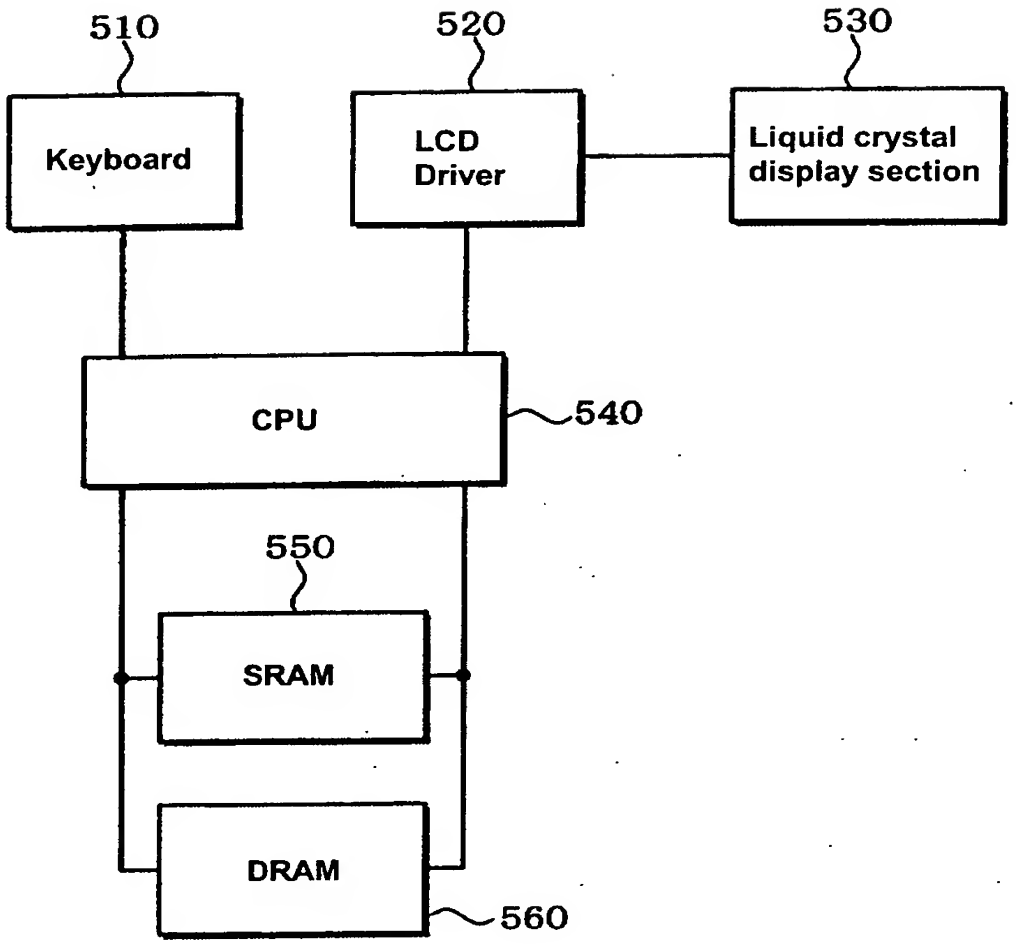
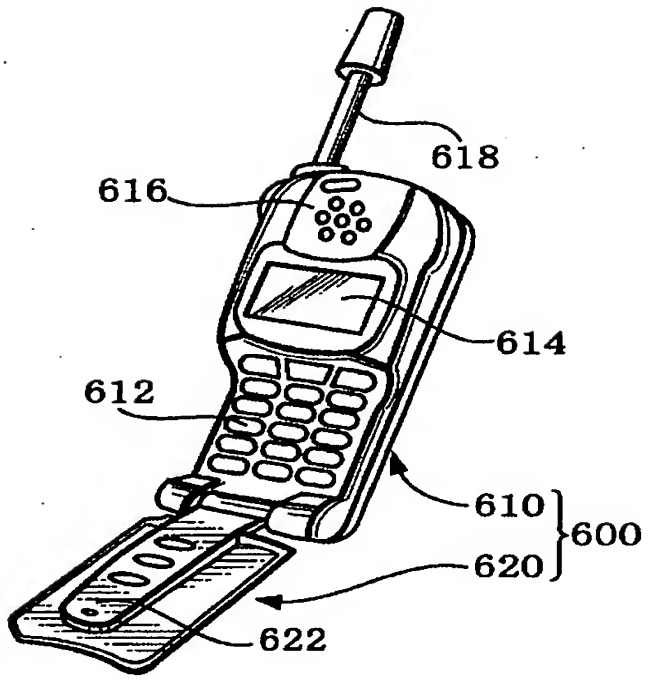

510
520
530
Keyboard
LCD Driver
Liquid crystal display section
CPU
540
550
SRAM
DRAM
560

Fig. 15



[Name of Document] ABSTRACT

[Abstract]

[Object] The present invention provides a semiconductor device that can reduce its cell area. The present invention further provides a memory system and an electronic apparatus that includes a semiconductor device of the present invention.

[Arrangement] A semiconductor device is provided with a memory cell including a first load transistor Q5, a second load transistor Q6, a first driver transistor Q3, a second driver transistor Q4, a first transfer transistor Q1 and a second transfer transistor Q2. The semiconductor device includes a first gate-gate electrode layer 20, a second gate-gate electrode layer 22, a first drain-drain wiring layer 40, a second drain-drain wiring layer 42, a first drain-gate wiring layer 30, and second drain-gate wiring layers 32a and 32b. The first drain-gate wiring layer 30 and the second drain-gate wiring layers 32a and 32b are located in different layers.

[Selected Figure] Fig. 1